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DISCLOSURE TITLE: MOS Gate Stack Rie Process With Self-Passivating Sidewalls

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DISCLOSURE TEXT:

- The gate stack in current MOS devices is defined by first **etching** through the stack, then overcoating with conformal Si3N4, and then **etching** off the Si3N4 (Fig. 1). This leaves Si3N4 covering the edges of the stack to passivate them. This publication describes a new method (Fig. 2) of forming a stack with passivated sidewalls which simplifies the process, improves process control tolerances, and reduces **etch**-induced damage. The key feature of the process is the use of a halosilicon gas in place of the more usual halocarbon gas, in combination with O2 . In a typical example, a CF4 + O2 process, the O2 leads to increased F production by reacting with the carbon to form CO2, which is pumped away. In the new process, using SiF4 + O2, the same increase in F is observed, but the reaction product of O2 and Si is SiOx which deposits on the surfaces of the wafer.

On the horizontal surfaces a competition then exists between oxide growth and ion bombardment-induced **etching**. The balance depends on the O2 concentration and the incident RF power. On the sidewalls, however, there is little or no ionic bombardment and the oxide growth process predominates. Experiments demonstrating this effect have been performed on WSix/ W/WSix stacks. Using CF4 + O2, severe undercuts appear in the WSix layers. When SiF4 + O2 is used,

vertical sidewalls are produced with no undercut. Further evidence is found in the dependence of **etch** rate on percent O2 in the SiF4 feed gas. At low power levels, the addition of O2 to the SiF4 results in a decrease in **tch** rate even though the F concentration (as measured by optical emission spectroscopy) increases roughly linearly with O2

At high power, on the other hand, the **etch** rate increases with O2 . These observations indicate that at low power, oxide growth competes with the **etching** process, while at high power, the higher level of ion bombardment dominates over oxide growth. In addition to the process simplification resulting from this approach to gate **etching,** there are other potential advantages: 1) The avoidance of carbon in the **etch** gas is expected to result in less contamination-induced degradation of device performance. 2) Control of the process is simplified compared to the Si3N4 **etching** process because of the higher **etch** rate ratio and the reduced concern over undercutting in the stack **etch** process.

The results described above relate specifically to SiF4, but other Si-F-Cl compounds should produce similar results, e.g., SiClF3, SiCl2F2, SiCl4, **Si2F6,** Si2Cl6, etc. This broadens the choices available for optimizing a specific gate **etching** process, and should permit use of this type of process for metal gates for submicron CMOS devices in the future.

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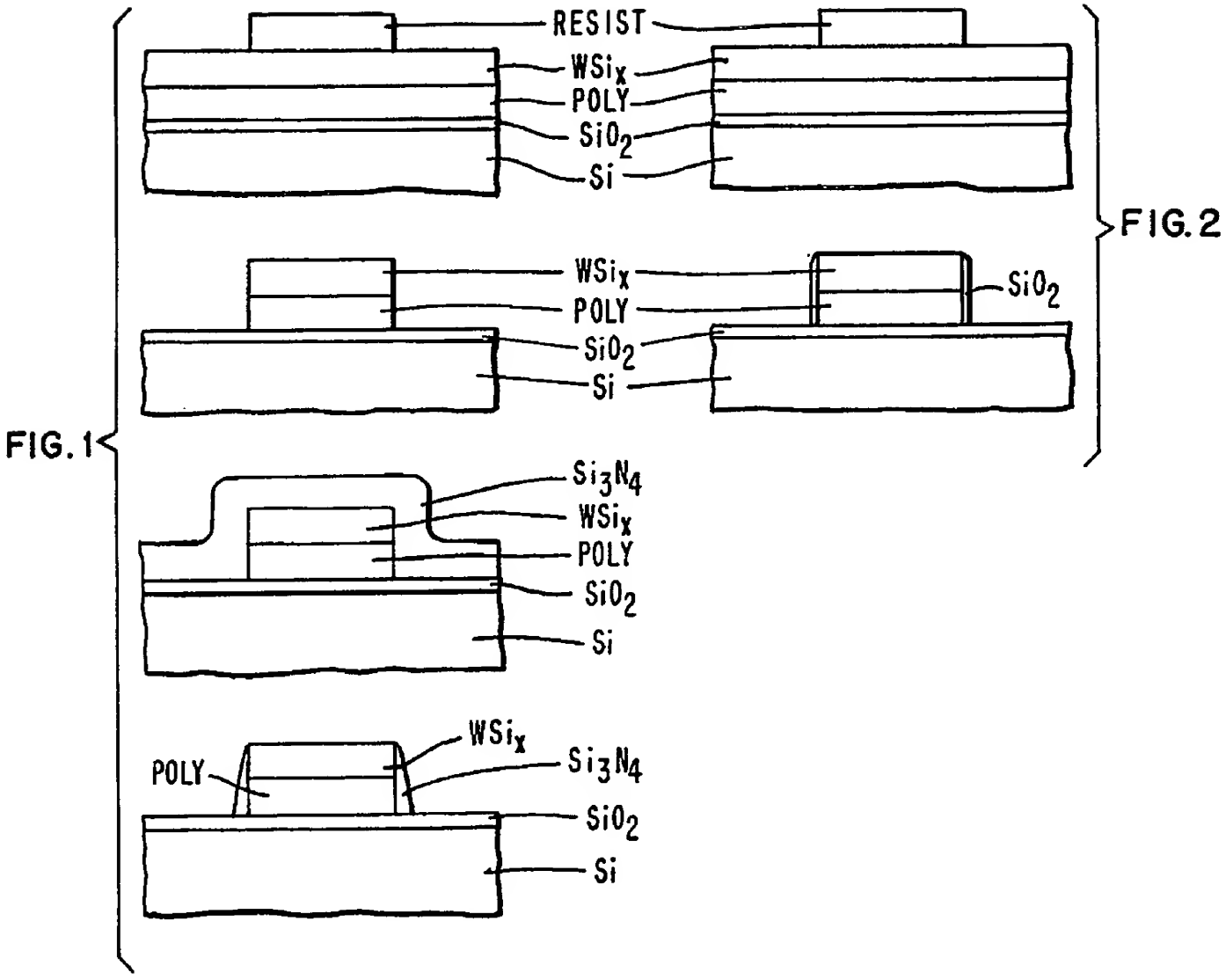
RESIST
WSix
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POLY
Si3N4
SiO2
Si

FIG. 1

FIG. 2